

Date: June 27, 2018

## EIC Detector R&D Progress Report and Proposal

**Project ID:** eRD18

**Project Name:** Precision Central Silicon Tracking & Vertexing for the EIC

**Period Reported:** January 1 to June 27, 2018

**Project Leader:** Peter Jones

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### Abstract

We propose to develop a detailed concept for a central silicon pixel detector for an Electron-Ion Collider at BNL or JLab exploring the advantages of depleted MAPS (DMAPS) in HV-/HR-CMOS technologies to achieve improved spatial resolution and timing capability over traditional MAPS. The sensor development will exploit the Birmingham Instrumentation Laboratory for Particle Physics and Applications. An accompanying simulation study will optimise the basic layout, location and sensor/pixel dimensions to find the best achievable momentum resolution and vertex reconstruction resolution. This initial design study will allow future full-detector simulations to explore precision measurements of heavy flavour processes and scattered electrons at high  $Q^2$ .

## 1. Report

### 1.1 What was planned for this period?

The project is divided into two work packages. WP1 focuses on sensor development and WP2 focuses on layout simulations. For this period the plan for WP1 was to continue the characterisation of the TowerJazz (TJ) investigator chip, fabricated in both the *standard* and *modified* processes, and to start the characterisation of test structures and prototypes available through our involvement in other DMAPS projects. We also planned to involve a chip designer to perform simulations at a schematic/layout level in order to explore possible readout architectures for a dedicated EIC DMAPS sensor. We are particularly interested in the timing requirements of such sensor and at the January meeting the Committee encouraged us to report on the feasibility of a possible outer timing layer. This study was to be informed by the detector layout simulations of WP2. The plan for WP2 was to define specifications for the sensors, by studying momentum resolution and impact parameter resolution in the transverse plane, based upon different assumptions for

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the number and radiation length of the barrel layers and pixel size. The impact of an additional timing layer has also been considered.

### *1.2 What was achieved?*

In this section we divide our report into two sections corresponding to the work packages defined above.

#### WP1 – Sensor development

During the past 6 months, work on WP1 has developed along two lines:

- further work on technology evaluation;
- definition of specifications for a dedicated EIC DMAPS sensors to start evaluation of readout architectures with a chip designer.

The technology evaluation has continued with the TJ test structures. A new investigator chip has become available at the beginning of the year. The design is largely based on the previous version with over 100 matrices of 10x10 pixels with different size of collection electrode and spacing between electronics and readout. This second implementation features a few modifications. The p-substrate and the p-well containing the electronics can be biased separately to allow for higher substrate bias and thus larger depletion and electric field. The 3T readout structure has been modified to allow for faster readout, in the order of a few ns, and the large pitch pixels have a reduced spacing between the electronics and the collection electrode to improve charge collection. In addition to this, the CERN ATLAS group has developed a fully monolithic DMAPS prototype in the modified TJ process, the MALTA sensor, which has recently become available (see table 1 for details). For the reasons explained below, we believe that the MALTA sensor is a good starting point to inform a DMAPS optimisation for the EIC, and we are starting to work with it.

Our project Ph.D. student, Håkan Wennlöf, has worked with CERN collaborators on irradiations and test beams of both the TJ investigator 2 chip and the MALTA sensor. He has carried out irradiations of the TJ investigator 2 chip at the MC40 cyclotron in Birmingham and he is preparing to start testing of the irradiated TJ investigator 2 chips. The test beam took place at CERN where he spent two weeks working on set up, data taking, and analysis. The results of the test beams are not yet public so we cannot present them in this report.

At the same time, we have been evaluating the characteristics of state-of-the-art DMAPS prototypes to identify a suitable development and optimisation path for a dedicated DMAPS sensor prototype for the EIC. Table 1 summarises the main features of state-of-the-art DMAPS prototypes in commercial HV/HR-CMOS technologies<sup>†</sup> [1]. These prototypes have been developed for application at the HL-LHC in the ATLAS experiment. They have been optimized to cope with high particle rates and radiation

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<sup>†</sup> We note that other technologies have also been investigated for DMAPS development (XFAB, ESPROS, Toshiba, Global Foundries, ST microelectronics, etc.). However, at the time of writing these have not reached a fully monolithic design and exist only at the level of test structures with partial readout capabilities. They are thus not considered in the Table 1.

Table 1: Comparison of state-of-the-art MAPS (ALPIDE [2]) and DMAPS sensors (MALTA [3,4], TJ-MONOPIX [5], LF\_MONOPIX [5], ATLASpix [6]), designed respectively for heavy ion and proton-proton experiments at LHC. The power figures of the ALPIDE sensor refer to the inner/outer layers of the ALICE ITS [10]. Due to their recent developments, some power figures of the DMAPS sensors are not yet published.

	ALPIDE	MALTA	TJ-MONOPIX	LF_MONOPIX	ATLASpix_Simple
Experiment	ALICE ITS	ATLAS ITk pixel Phase II (outermost layers only)			
Technology	TJ 180 nm	Modified TJ 180 nm		LF 150 nm	AMS 180 nm
Substrate resistivity [kOhm cm]	> 1 (epi-layer 18-25 um)			> 2	0.08 - 1
Collection electrode	small	small	small	large	large
Detector capacitance [fF]	<5			Up to 400	
Chip size [cm x cm]	1.5 x 3	2 x 2	1 x 2	1 x 1	0.325 x 1.6
Pixel size [um x um]	28 x 28	36.4 x 36.4	36 x 40	50 x 250	40 x 130
Integration time [ns]	4 x 10 <sup>3</sup>	<25			
Particle rate [kHz/mm <sup>2</sup> ]	10	10 <sup>3</sup>			
Readout architecture	Asynchronous		Synchronous, column drain		
Analogue power [mW/cm <sup>2</sup> ]	5.4	< 120	~ 110	~ 300	N/A
Digital power [mW/cm <sup>2</sup> ]	31.5/14.8	N/A	N/A	N/A	N/A
Total power [mW/cm <sup>2</sup> ]	36.9/20.2	N/A	N/A	N/A	N/A
NIEL [1MeV n <sub>eq</sub> /cm <sup>2</sup> ]	1.7 x 10 <sup>13</sup>	1.0 x 10 <sup>15</sup>			
TID [Mrad]	2.7	50			

levels and achieve a time resolution in the order of few tens of ns. Comparing the pixel sizes and available power consumption figures for the current developments, it appears that a DMAPS sensor for the EIC would benefit from having a small collection electrode as this allows for small pixel pitch and low power analogue FE design. Full depletion should also be achieved and a suitable HV/HR-CMOS technology needs to be identified. Of the surveyed technologies, the TJ modified process is the only one providing full depletion with a small collection electrode thanks to the introduction of a deep planar junction [9]. Asynchronous readout would have the potential of matching the same timing and rate requirements with a lower digital power consumption with respect to synchronous architectures and, thus, would be the preferred option.

Starting from these considerations a set of initial specifications can be compiled for an EIC DMAPS sensor. These are summarised in table 2. Two sets of specifications are collected, one for the vertex and tracking detector and one for an outer layer providing fast timing to tag bunch crossings. Different design optimisations might be needed for the inner radii, which require very small pixel size and very low material, and for the larger radii, where time stamping capability could be added at the expense of slightly larger pixels and increased material. This would most certainly be the case for an EIC at JLAB as the bunch crossing frequency would require an integration time of the order of the ns. For eRHIC, an integration time of the order of 100 ns could possibly be achieved for all layers so that the same DMAPS sensor could be used for tracking, vertexing and timing. It is worth mentioning at this point that the DMAPS designs considered for the central silicon tracker could also be used for the forward and backward silicon trackers.

Simulations have started to inform the requirements in terms of pixel size and material at different radii to understand where time stamping capability could be added, without degrading the impact parameter resolution or the momentum resolution. Results on these investigations are reported below in WP2.

Table 2: Initial specifications for an EIC DMAPS sensor. An interaction rate of 500kHz is assumed to derive the integration time for the vertex and tracking detector [7]. The integration time for the timing detector assumes bunch crossing frequencies of 9.38 MHz for eRHIC and 748.5 MHz MEIC, and that each bunch crossing needs to be tagged as this would be the worst case [8].

	EIC DMAPS sensor	
	Vertex and tracking	Outer timing layer
Detector	TJ or similar	
Technology	TJ or similar	
Substrate resistivity [kOhm cm]	> 1	
Collection electrode	small	
Detector capacitance [fF]	<5	
Chip size [cm x cm]	Reticule size [cm <sup>2</sup> ]	
Pixel size [um x um]	20 x 20	TBD
Integration time [ns]	<2 x 10 <sup>3</sup>	< 100 (eRHIC) <1 (MEIC)
Particle rate [kHz/mm <sup>2</sup> ]	TBD	
Readout architecture	Asynchronous	TBD
Analogue power [mW/cm <sup>2</sup> ]	TBD	TBD
Digital power [mW/cm <sup>2</sup> ]	TBD	TBD
Total power [mW/cm <sup>2</sup> ]	TBD	TBD
NIEL [1MeV n <sub>eq</sub> /cm <sup>2</sup> ]	10 <sup>10</sup>	
TID [Mrad]	TBD	

## WP2 – Detector layout simulations

Layout simulations have been based upon the BeAST detector concept, modelled using GEANT in the EicRoot framework. The central tracker is comprised of a compact Time Projection Chamber (TPC: outer tracker) and a multi-layer silicon vertex tracker (VST: inner tracker). The radius of the TPC inner field cage is assumed to be 20 cm. The default VST geometry is a four-layer device comprising two inner layers, close to the beryllium beampipe, and two outer layers, close to the TPC inner field cage. This minimal layout provides redundancy (i.e. two sense layers at each location) while simultaneously minimising uncertainties associated with the propagation of tracks from the outer tracker onto the outermost silicon tracker layers and maximising the pointing resolution by locating the innermost layers as close as possible to the beampipe. All our simulations assume that each of the two inner silicon tracking layers have a thickness of  $0.3\% X/X_0$  and that the outer two layers have a thickness of  $0.8\% X/X_0$ . This is based on the specifications of the ALICE ITS inner and outer barrel layers, respectively. In addition to the default 4-layer device, we have also investigated the impact of adding a fifth outer *timing* layer. Here, we are working under the assumption that the tracking layers will not provide sufficient time resolution to timestamp individual bunch crossings. The additional timing layer is assumed to provide a faster readout rate, albeit with perhaps slightly poorer spatial resolution (larger pixels) and higher power density. The timing layer is therefore assumed to contribute  $1.6\% X/X_0$  to accommodate the requirement for increased cooling and services (e.g. power cables). The aim has been to investigate the impact of the timing layer on the momentum resolution and impact parameter resolution measured at the interaction point. A schematic diagram showing the arrangement of the inner and outer trackers is shown in Fig. 1.

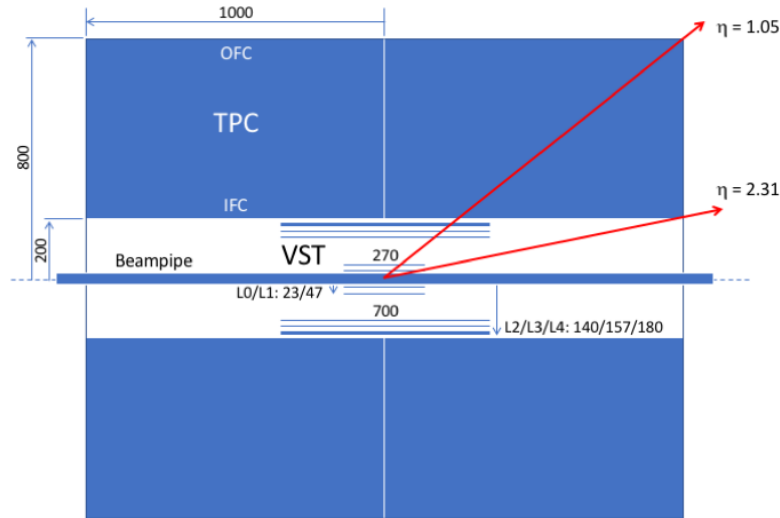


Figure 1. Simulation layout (dimensions in mm). The VST inner tracking layers are labelled L0 and L1. The outer layers and optional timing layer are labelled L2, L3 and L4, respectively.

The physics measurement that places strongest constraints on the performance of the inner tracking system is the reconstruction of open charm decays. To this end, we have simulated charm meson production in e-p collisions at  $\sqrt{s} = 31.6, 63.2$  and  $141.4$  GeV using Pythia, corresponding to electron beam energies of 5, 10 and 20 GeV and

proton beam energies of 50, 100 and 250 GeV, respectively. This has shown that the mean transverse momentum of the decay daughters is  $\langle p_T \rangle \lesssim 1 \text{ GeV}/c$ . Our simulations have therefore been performed with charged pions in the range  $0 \leq p_T \leq 5 \text{ GeV}/c$ , covering the pseudorapidity interval  $-1 \leq \eta \leq 1$ , where there is full coverage by the outer tracker. A uniform solenoidal magnetic field of field strength  $B = 1.5 \text{ Tesla}$  is assumed. This corresponds to a minimum transverse momentum threshold of  $p_T \geq 0.24 \text{ GeV}/c$  for tracks that reach the TPC Outer Field Cage. Below this value, tracks will spiral in the TPC. Currently, nothing is done to account for these spiralling tracks. In the simulations we have studied combined VST+TPC tracks, unless otherwise stated.

Fig. 2 shows the relative momentum resolution and transverse pointing resolution for the 4-layer default VST configuration as a function of transverse momentum for three choices of pixel size:  $20 \times 20 \mu\text{m}^2$ ,  $30 \times 30 \mu\text{m}^2$  and  $40 \times 40 \mu\text{m}^2$ . The results show that the spatial resolution of the silicon tracker has a negligible effect on the momentum resolution, the momentum resolution being determined primarily by the total track length, whereas the 2d pointing resolution in the transverse plane (distance of closest approach to the interaction point) is improved with smaller pixels. In this case, the resolution is driven by the spatial resolution of the innermost layer, achieving a  $20 \mu\text{m}$  pointing resolution at  $1 \text{ GeV}/c$  for the smallest pixel size studied here.

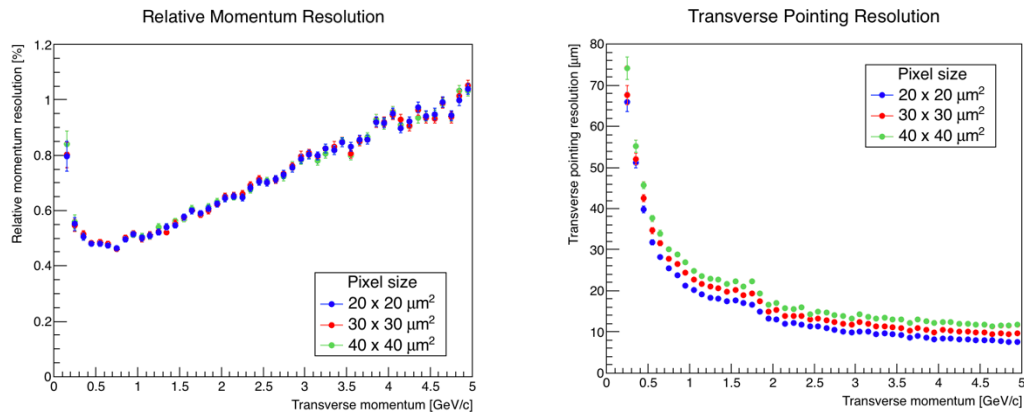


Figure 2. Relative momentum resolution ( $\sigma_{p_T}/p_T$ ) (left) and transverse pointing resolution (right) as a function of transverse momentum for three choices of pixel size.

Fig. 3 shows a comparison of the relative momentum resolution and transverse pointing resolution for the 4-layer default VST configuration as a function of transverse momentum with TPC-only tracks. In this simulation, the pixel size of the VST layers is chosen to be  $20 \times 20 \mu\text{m}^2$ . The improvement due to the addition of the VST is clearly seen in both cases.

Fig. 4 shows an attempt to parametrise the relative momentum resolution and transverse pointing resolution for the 4-layer default VST configuration as a function of transverse momentum. In this simulation, the pixel size of the VST layers is chosen to be  $20 \times 20 \mu\text{m}^2$ . The relative momentum resolution is parameterised with a function of the form

$$\frac{\sigma_{p_T}}{p_T} = \sqrt{p_0^2 + (p_1 \cdot p_T)^2}.$$

The transverse pointing resolution is parameterised with a function of the form

$$\sigma_{DCA2d}(\mu m) = \sqrt{p_0^2 + \left( \frac{p_1 \cdot 1 \text{ GeV/c}}{p_T} \right)^2}.$$

In both cases,  $p_0$  and  $p_1$  are fit parameters. The pointing resolution is quite well described over the full range of transverse momentum. However, the function for the momentum resolution does not account for multiple scattering at low transverse momentum. Nevertheless, both functions provide a convenient method for evaluating the performance of different tracker geometries.

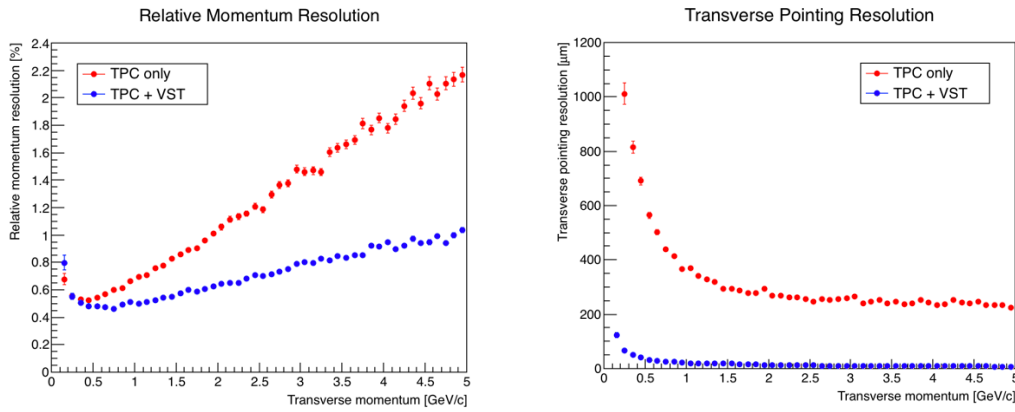


Figure 3. Relative momentum resolution ( $\sigma_{p_T}/p_T$ ) (left) and transverse pointing resolution (right) as a function of transverse momentum comparing VST+TPC tracks with TPC only tracks. The pixel size of VST layers is chosen to be  $20 \times 20 \mu m^2$ .

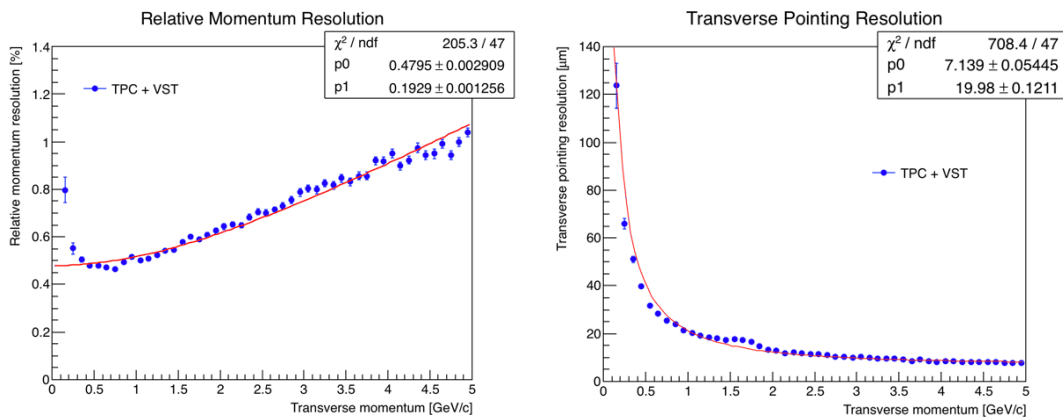


Figure 4. Relative momentum resolution ( $\sigma_{p_T}/p_T$ ) (left) and transverse pointing resolution (right) as a function of transverse momentum for VST+TPC tracks. The pixel size of VST layers is chosen to be  $20 \times 20 \mu m^2$ . An attempt has been made to parametrise the function form of the distributions (see text for details).

Finally, Fig.5 show a comparison of the relative momentum resolution and transverse pointing resolution for the 4-layer default VST configuration as a function of transverse momentum with the 5-layer option incorporating a 1.6%  $X/X_0$  outer timing layer. It should be noted that the pixel size of all VST layers, including the timing layer, was chosen to be  $20 \times 20 \mu\text{m}^2$  in this simulation. The results show that the additional silicon layer introduces a minor degradation in momentum resolution above  $p_T = 2 \text{ GeV}/c$ . However, it has a negligible impact on pointing resolution except for tracks below  $p_T = 0.5 \text{ GeV}/c$ .

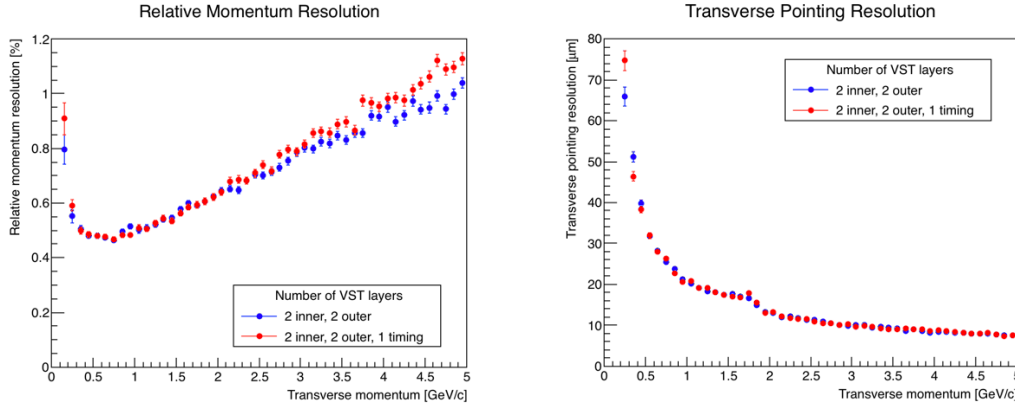


Figure 5. Relative momentum resolution ( $\sigma_{p_T}/p_T$ ) (left) and transverse pointing resolution (right) as a function of transverse momentum for VST+TPC tracks with and without an additional silicon timing layer. The pixel size of all VST layers (including the timing layer) is chosen to be  $20 \times 20 \mu\text{m}^2$ .

In summary, the simulations studies in WP2 have shown that pointing resolution is a function of the spatial resolution of the innermost silicon tracking layer. The momentum resolution is rather insensitive to the spatial resolution of the pixel layers but, comparing TPC only tracks and TPC+VST tracks, it is dependent upon the overall reconstructed track length and therefore benefits from the larger lever arm provided by the inner most VST layers. An additional tracking layer, with a total thickness equal to that of the outer two tracking layers has been shown to have a minor negative impact on the performance of the combined TPC+VST tracker.

### 1.2 What was not achieved, why not, and what will be done to correct?

Work with a chip designer on investigating possible readout architectures for an EIC DMAPS prototype planned for this period has not started as a set of initial specifications needed to be defined. These are now becoming available via the WP2 simulations and the survey and evaluation of current DMAPS technologies, so we plan to start this work in the next six months and report initial progress in January. This work will complement the detector layout simulations of WP2 and inform the definition of the DMAPS specifications.

*1.4 What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?*

The answer to this question is covered in the Proposal section below.

*1.5 What are critical issues?*

The DMAPS technology available from TJ appears to be the best option at the current time and already meets most of the requirements of a future EIC detector. The only outstanding question concerns the timing performance, which requires careful optimisation of the in-pixel electronics. Timing considerations have been part of our technology evaluation and will be pursued further in our proposed programme of work for the next period.

## 2. Proposal

### *2.1 Introduction*

Our proposal for the next funding period (FY19) builds upon our original proposal and remains focused on the design of a precision central silicon tracking and vertex detector for a future EIC detector. The relevance for the EIC is high precision tracking and the identification of secondary vertices in the central region. As such, the requirements for the detector are driven by the reconstruction of displaced vertices from the decay of charmed and beauty hadrons. The focus of the EIC physics programme on the role of gluons in the structure of hadrons places a strong emphasis on heavy flavour observables. Heavy flavour production is directly sensitive to the gluon density in the hadron beam at lowest order as well as probing a wide range of issues in perturbative QCD. Similarly, the use of heavy flavours as probes of deconfinement in relativistic heavy-ion collisions provides further motivation to study the same observables in e+A collisions, where cold nuclear matter effects can be explored. Open charm production in polarised e+p scattering has also provided insight into the role of gluons in determining the spin structure of the proton. These points are fully recognised in the EIC White Paper [8] but there is no detailed study to date which looks closely at the optimization of the central silicon tracker layout to address this physics.

### *2.2 Proposed programme of work*

As highlighted in our last proposal, there are clear synergies between the aims of this project and eRD16, which is concerned with forward/backward tracking. eRD16 has already shown that there are some interesting and potentially important integration and performance issues relating to the interface between the barrel and the first planes of disks, closest to the IP. At low and high x, heavy flavour production will be in the forward/backward regions, underlining the need for a unified approach. We will therefore continue to work with eRD16 to iterate towards a final inner silicon detector design incorporating both the barrel and the forward/backward disks. This proposal

also has an emphasis on sensor R&D and will seek to define the capability of the technology to meet the requirements coming from the simulations.

Following the work package breakdown structure of our original proposal, our proposed programme of work for the next period is divided into two work packages: WP1 on sensor development and WP2 on detector layout investigations.

### *2.2.1 WP1: Sensor development*

The scope of WP1 is evolving with respect to the original plan following the developments of the first two years. The initial proposal aimed at evaluating the advantages of charge collection by drift in depleted MAPS over traditional MAPS in order to achieve higher spatial resolution. We had proposed different ways of achieving full depletion, via technology modifications or multi-electrode/large electrode pixel layouts, based on test structures and prototypes available to us via other R&D projects. We now concentrate only on the TJ 180 nm modified process as it allows to design fully depleted MAPS with small collection electrode, a suitable configuration for an EIC DMAPS sensor. In FY19 we thus plan to continue evaluation of the TJ investigator 2 chip and possibly of the MALTA sensor. We will not pursue any further the evaluation of structures from our DECAL and RD50 projects as they feature respectively multiple collection electrodes and large collection electrode that would lead to higher pixel capacitance and thus larger pixels and higher power consumption.

In addition to this, we now understand that the EIC would benefit of a DMAPS sensor with improved integration time with respect to ALPIDE, and that timing-wise the ultimate goal of this technology would be to time stamp the bunch crossings where the primary interaction occurred [7]. This broadens the scope of WP1 to include work on the study of possible readout architectures able to accommodate the required timing performance while matching the required vertex and momentum resolution. The addition of time stamping capability might necessitate an outer timing layer with higher granularity. This development would bring possible synergies with colleagues from eRD6 consortia as they propose to implement a timing layer between silicon and TPC. Their proposal assumes ALPIDE for the silicon part so they are looking at implementing this timing layer with  $\mu$ RWELL technology.

As a candidate technology and a first set of specifications has been defined we would like to start working with a chip designer and evaluate different readout architectures to match the EIC timing requirements. One figure that is still needed is the particle rate as this is a fundamental input to define the readout scheme. We will iterate with our colleagues from eRD16 who have started working on this and already shown results at previous meetings, and with Alexander Kiselev and colleagues working on the EIC detector simulation. The pixel readout could be carried out in collaboration with BNL's instrumentation division who have also expressed an interest in developing a DMAPS prototype for the EIC in a different technology. Sharing a common set of specifications and discussing readout architectures and technology performance will allow us to identify the most promising technology to take forward. In January, we would like to present the committee with an updated list of specifications developed

in collaboration with the above-mentioned partners and possibly some first example of readout architecture that could be implemented in TJ.

To this aim, we will continue to work closely with eRD16 over the next funding period, holding monthly phone meetings to progress the work on defining the pixel chip specifications and evaluating the readout architecture. We also propose to hold face-to-face meetings twice a year, ideally in anticipation of R&D meetings. Going forward, the aim would be to form a consortium that combines Birmingham's expertise in silicon detectors development and LBNL's expertise on mechanical design and services. The first job of the consortium should be to draw up a prioritised list of elements of the silicon tracker design that require targeted R&D.

### 2.2.2 WP2: Detector layout investigations

Preliminary investigations of e-p collisions at  $\sqrt{s} = 31.6, 63.2$  and  $141.4$  GeV using Pythia have shown that charm mesons are produced over a typically wide range in pseudorapidity. This is illustrated in Fig. 6 below, which shows  $D^0$  pseudorapidity distribution at  $\sqrt{s} = 141.4$  GeV (20 GeV x 250 GeV). The full radial coverage of the central tracker (VST+TPC) is shown by the blue shaded region. The red shaded region shows where there is partial coverage by the outer track (TPC) where the placement of the first forward/backward disks may enable charm reconstruction, albeit with lower resolution due to shorter track lengths. We therefore propose studying the placement of the innermost forward/backward disks within the outer VST layers (see Fig.1 for reference).

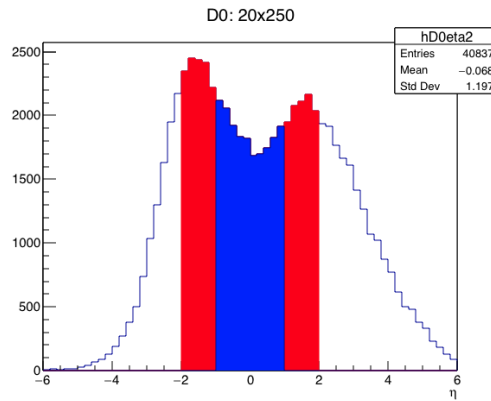


Figure 6. The pseudorapidity distribution of  $D^0$  mesons in e-p collisions at  $\sqrt{s} = 141.4$  GeV. The electrons are travelling in the negative pseudorapidity direction. The shading corresponds to the full (blue) and partial (red) coverage of the outer tracker.

In order to optimise the radial position of the VST layers, consideration must be given to track propagation errors. It is assumed that track candidates will be reconstructed in the TPC, or outer tracker, first and then propagated inwards. The radial position of the layers depends upon the projected search area and the average hit density given the integration time of the pixels, which may be significantly longer than the inter bunch spacing, particularly at JLEIC. Some development of the EicRoot package is needed to achieve this and we propose to work with Alexander Kiselev to find a solution to the problem. Beyond this, we can start to think about tracking algorithms and searching for displaced vertices in full events.

The specific questions we wish to address are:

- How many layers are needed and at what radii?
- What is the optimal length of the barrel layers and what overlap in acceptance with the forward/backward disks is possible/desirable?
- To what extent is it possible to identify displaced vertices in full events?

### 2.3 Request for resources

Wherever possible existing resources will be devoted to the project. This includes academic time (see Personnel), computing resources and consumables. The University of Birmingham provides funds to support a 3.5-year Ph.D. studentship, which was taken up by Håkan Wennl f in October 2017. In fact, most of the work presented in this proposal is his. The majority of the work proposed in WP2 will therefore be carried out using existing resources.

In FY18, we made a request for PDRA support, which was partially funded. We subsequently asked the Committee to permit us to use the money to employ a chip designer to do some preliminary electronic design evaluations. This amounted to \$84k, which would pay for 4-6 months of designer time at the Rutherford Appleton Laboratory (RAL). As explained in our report, this part of our FY18 award has not yet been spent, but our plan is to use it in the second half of 2018 and we will report our initial findings at the January meeting. For FY19, we are requesting an additional 3-4 months of designer time (\$60k), plus a modest amount (\$6k) to pay for new readout boards to enable us to evaluate the TJ investigator 2 and MALTA chips in Birmingham, plus travel (\$14k) to enable participation at EIC meetings and collaboration with LBNL (eRD16) on defining the basic layout, finalising the pixel chip specifications and evaluating the readout architecture, as outlined in our proposal.

In summary, the requested level of funding is:

1. Additional 3-4 months of chip designer time at RAL	\$60,000
2. Readout equipment (FPGA board, external amplifier, cable)	\$6,000
3. Travel (4 x 2 x £1,250)	\$14,000
<b>Total</b>	<b>\$80,000</b>

The requested amount (\$80k) is nearly 20% lower than awarded in FY18 and represents the optimal level of funding. Descope options of -20% and -40% would result in a loss of designer time (see Table 3). In these scenarios, we would choose to prioritise our ability to perform technology evaluations in Birmingham, plus travel to facilitate collaboration with LBNL and the wider EIC community.

Table 2: FY19 cost breakdown for the three funding scenarios.

Scenario	Chip designer	Equipment	Travel	Total (USD)
100%	\$60,000	\$6,000	\$14,000	\$80,000
80%	\$44,000	\$6,000	\$14,000	\$64,000
60%	\$28,000	\$6,000	\$14,000	\$48,000

### 3. Personnel

*Include a list of the existing personnel and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located and who supervised their work.*

Prof. Peter Jones (0.05 FTE) – no cost

Dr. Laura Gonella (0.1 FTE) – no cost

Håkan Wennlöf – (1 FTE) – no cost

Prof. Phil Allport and Prof. Paul Newman have an advisory role and participate in our regular project meetings to monitor progress.

### 4. External Funding

*Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.*

The University of Birmingham provides the Ph.D. studentship that supports Håkan Wennlöf.

### 5. Publications

*Please provide a list of publications coming out of the R&D effort.*

None at this stage of the project.

### References

- [1] N. Wermes, CMOS detectors development, RD50 meeting, <https://indico.cern.ch/event/719814/contributions/3022652/>, June 2018.
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